IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-10 (Canceled):

Claim 11 (Currently Amended): A semiconductor integrated circuit device, comprising:

a semiconductor substrate with an active region defined by an element isolation region, word lines extending in a first direction over said active region such that gate electrodes of metal insulator semiconductor field effect transistors (MISFETs) are electrically coupled to said word lines, semiconductor regions formed in said active region extending in a second direction perpendicular to the first direction such that said semiconductor regions serve as a source region or a drain region of each MISFET;

a first insulating film and a second insulating film covering said active region, said word lines and said semiconductor regions;

a first opening formed in said first insulating film such that said first opening is arranged between said word lines and extends, in said first direction, from a semiconductor region to said element isolation region;

a second opening formed in said second insulating film under said first opening such that a diameter of said second opening in said first direction is less than that of said first opening, and such that said second opening reaches said semiconductor regions;

a conductive material buried in said first opening and in said second opening; and

a bit line formed on said first opening ~~which is formed on said second insulating film~~ such that said bit line is electrically coupled to said conductive material and extends to cross said word lines,

wherein one end portion of said first opening in said first direction is formed on said second opening and over said semiconductor region, and is not covered with said bit line, and

wherein another end portion of said first opening in said first direction is formed on said second insulating film, over said element isolation region and under said bit line.

Claim 12 (Previously Presented): A semiconductor integrated circuit device according to claim 11, further comprising:

a capacitor element formed over said first insulating film;

a third opening formed in said first insulating film and said second insulating film to reach other semiconductor region; and

a conductive material buried in said third opening,

wherein said capacitor element is electrically coupled to the other semiconductor region through said conductive material buried in said third opening.

Claim 13 (Original): A semiconductor integrated circuit device according to claim 12, wherein a memory cell of a dynamic random access memory is comprised of said MISFET and said capacitor element.

Claim 14 (Currently Amended): A semiconductor integrated circuit device, comprising:

a semiconductor substrate provided with an active region defined by an element isolation region, word lines extending in a first direction over said active region extending in a second direction perpendicular to the first direction such that gate electrodes of metal insulator semiconductor field effect transistors (MISFETs) are electrically coupled to said word lines, semiconductor regions formed in said active region such that said semiconductor regions serve as a source region or a drain region of each MISFET;

a first insulating film and a second insulating film deposited over said active region, said word lines and said semiconductor regions;

a first opening formed in said first insulating film such that said first opening is arranged between said word lines and extends, in said first direction, from a semiconductor region to said element isolation region;

a second opening formed in said second insulating film under said first opening such that a diameter of said second opening in said first direction is less than that of said first opening, and such that said second opening reaches said semiconductor region;

a third opening formed in said first insulating film and said second insulating film to reach other semiconductor region;

a conductive material buried in said first opening, said second opening, and said third opening; and

a bit line formed on said first opening ~~which is formed on said second insulating film~~ such that said bit line is electrically coupled to said conductive material and extends to cross said word lines,

wherein one end portion of said first opening in said first direction is formed on said second opening and over said semiconductor region, and is not covered with said bit line, and

wherein another end portion of said first opening in said first direction is formed on said second insulating film, over said element isolation region and under said bit line.

Claim 15 (Previously Presented): A semiconductor integrated circuit device according to claim 14, further comprising:

a capacitor element formed over said first insulating film,

wherein said capacitor element is electrically coupled to said other semiconductor region through said conductive material buried in said third opening.

Claim 16 (Previously Presented): A semiconductor integrated circuit according to claim 14, wherein a memory cell of a dynamic random access memory is comprised of said MISFET and said capacitor element.

Claim 17 (Currently Amended): A semiconductor integrated circuit device comprising:

a semiconductor substrate with an active region defined by an element isolation region, word lines extending in a first direction over said active region such

that gate electrodes of metal insulator semiconductor field effect transistors (MISFETs) are electrically coupled to said word lines, semiconductor regions formed in said active region extending in a second direction perpendicular to the first direction, such that said semiconductor regions serve as a source region or a drain region of each MISFET;

a first insulating film covering said active region, said word lines and said semiconductor regions;

a first opening formed in said first insulating film, such that said first opening is arranged between said word lines and extends, in said first direction, from a semiconductor region to said element isolation region, and such that said first opening reaches said semiconductor region;

a conductive material buried in said first opening; and

a bit line formed on said first opening ~~which is formed on said element isolation region~~, such that said bit line is electrically coupled to said conductive material and extends to cross said word lines,

wherein one end portion of said first opening in said first direction is formed on said second opening and over said semiconductor region, and is not covered with said bit line, and

wherein another end portion of said first opening in said first direction is formed on said second insulating film, over said element isolation region and under said bit line.

Claim 18 (Previously Presented): A semiconductor integrated circuit device according to claim 17, wherein a memory cell of a dynamic random

access memory is comprised of said MISFET and a capacitor element formed over said first insulating film.